

CLAIMS

1 1. (currently amended) A programmable device comprising a Serial Peripheral Interface
2 (SPI) adapted to be connected in parallel to an SPI interface of ~~at least one~~ each of two or more SPI serial
3 memory devices such that the programmable device is adapted to receive a different portion of
4 configuration data stored in ~~[[the]]~~ each SPI serial memory device without transmitting the configuration
5 data via a controller connected between the SPI serial memory devices and the programmable device.

1 2. (currently amended) The invention of claim 1, wherein:
2 the programmable device is an FPGA; and
3 ~~[[the]]~~ each SPI serial memory device is an SPI serial flash PROM.

1 3. (currently amended) The invention of claim 1, wherein the programmable device is
2 adapted to independently generate at least one command adapted to control operations of ~~[[the]]~~ each SPI
3 serial memory device during configuration of the programmable device.

1 4. (currently amended) The invention of claim 1, wherein the programmable device is
2 adapted to generate a message to inform ~~[[the]]~~ each SPI serial memory device of a starting address to be
3 used to transfer the configuration data stored in ~~[[the]]~~ said each SPI serial memory device to the
4 programmable device.

1 5. (currently amended) The invention of claim 1, wherein the programmable device is
2 adapted to receive instructions to ignore data from ~~[[an]]~~ at least one of the SPI serial memory devices.

1 6. (original) The invention of claim 5, wherein the programmable device is adapted to
2 retrieve the instructions from the configuration data.

1 7. (canceled)

1 8. (currently amended) The invention of claim ~~[[7]]~~ 1, wherein the programmable device is
2 adapted to be instructed, based on information contained in the configuration data, as to how to interpret
3 the different portions of the configuration data received from the different SPI serial memory devices.

1 9. (currently amended) The invention of claim ~~[[7]]~~ 1, wherein the programmable device is
2 adapted to process different amounts of configuration data received from different SPI serial memory
3 devices.

1 10. (original) The invention of claim 9, wherein the two or more different SPI serial
2 memory devices are of two or more different sizes capable of storing the different amounts of the
3 configuration data.
4

1 11. (original) The invention of claim 9, wherein the programmable device is adapted to stop
2 including data from an SPI serial memory device that has already transmitted all of its configuration
3 data.

1 12. (currently amended) The invention of claim ~~[[7]]~~ 1, wherein the programmable device
2 comprises:
3 a multiplexer (mux) adapted to interleave the configuration data from the two or more different
4 SPI serial memory devices; and

5 a timing controller adapted to control the operations of the mux and to generate a configuration
6 clock signal used to control the timing of the reading of the configuration data from the two or more
7 different SPI serial memory devices.

1 13. (original) The invention of claim 12, wherein the timing controller is adapted to (1)
2 change the operations of the mux and (2) change the rate of the configuration clock signal, when the
3 number of SPI serial memory devices having configuration data to transmit changes.

1 14. (currently amended) The invention of claim [[7]] 1, wherein each different portion of
2 the configuration data from the corresponding SPI serial memory device is received at a different
3 configuration data input pin of the SPI interface of the programmable device.

1 15. (currently amended) The invention of claim [[7]] 1, wherein each of one or more output
2 pins of the programmable device is adapted to be connected to corresponding pins of all of the SPI serial
3 memory devices.

1 16. (original) The invention of claim 15, wherein the programmable device has a
2 configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins
3 of all of the SPI serial memory devices such that configuration data is transmitted simultaneously from
4 all of the SPI serial memory devices to the programmable device.

1 17. (currently amended) An apparatus comprising:
2 a programmable device having a Serial Peripheral Interface (SPI); and
3 ~~at least one~~ two or more SPI serial memory devices, each having an SPI interface, wherein:
4 the SPI interface of the programmable device is connected in parallel to the SPI
5 interfaces of the SPI serial memory devices such that the programmable device is adapted to receive a
6 different portion of configuration data stored in ~~[[the]]~~ each different SPI serial memory device without
7 transmitting the configuration data via a controller connected between the SPI serial memory devices and
8 the programmable device.

1 18. (currently amended) A method for configuring a programmable device, comprising:
2 reading a different portion of configuration data from a Serial Peripheral Interface (SPI) of ~~at~~
3 ~~least one~~ each of two or more different SPI serial memory devices connected in parallel to an SPI
4 interface of the programmable device without transmitting the configuration data via a controller
5 connected between the SPI serial memory devices and the programmable device; and
6 configuring the programmable device using the configuration data.

1 19. (currently amended) A programmable device adapted to be connected simultaneously in
2 parallel to two or more memory devices such that the programmable device is adapted to receive
3 configuration data stored in the two or more memory devices without transmitting the configuration data
4 via a controller connected between any of the memory devices and the programmable device, wherein
5 the programmable device is adapted to receive a different portion of the configuration data from each
6 different memory device.

1 20. (original) The invention of claim 19, wherein:
2 the programmable device has an SPI interface;
3 each memory device is an SPI serial memory device having an SPI interface; and
4 the SPI interface of each SPI serial memory device is connected to the SPI interface of the
5 programmable device.

1 21. (original) The invention of claim 19, wherein the programmable device is adapted to
2 independently generate at least one command adapted to control operations of the memory devices
3 during configuration of the programmable device.

1 22. (original) The invention of claim 19, wherein the programmable device is adapted to
2 generate a message to inform the memory devices of a starting address to be used to transfer the
3 configuration data stored in the memory devices to the programmable device.

1 23. (original) The invention of claim 19, wherein the programmable device is adapted to
2 receive instructions to ignore data from a memory device.

1 24. (original) The invention of claim 23, wherein the programmable device is adapted to
2 retrieve the instructions from the configuration data.

1 25. (original) The invention of claim 19, wherein the programmable device is adapted to be
2 instructed, based on information contained in the configuration data, as to how to interpret the different
3 portions of the configuration data received from the different memory devices.

1 26. (original) The invention of claim 19, wherein the programmable device is adapted to
2 process different amounts of configuration data received from different memory devices.

1 27. (original) The invention of claim 26, wherein the two or more different memory devices
2 are of two or more different sizes capable of storing the different amounts of the configuration data.

1 28. (original) The invention of claim 26, wherein the programmable device is adapted to
2 stop including data from a memory device that has already transmitted all of its configuration data.

1 29. (original) The invention of claim 19, wherein the programmable device comprises:
2 a multiplexer (mux) adapted to interleave the configuration data from the two or more different
3 memory devices; and
4 a timing controller adapted to control the operations of the mux and to generate a configuration
5 clock signal used to control the timing of the reading of the configuration data from the two or more
6 different memory devices.

1 30. (original) The invention of claim 29, wherein the timing controller is adapted to (1)
2 change the operations of the mux and (2) change the rate of the configuration clock signal, when the
3 number of memory devices having configuration data to transmit changes.

1 31. (original) The invention of claim 19, wherein each different portion of the configuration
2 data from the corresponding memory device is received at a different configuration data input pin of the
3 programmable device.

1 32. (original) The invention of claim 19, wherein each of one or more output pins of the
2 programmable device is adapted to be connected to corresponding pins of all of the memory devices.

1 33. (original) The invention of claim 32, wherein the programmable device has a
2 configuration clock signal pin adapted to be connected to corresponding configuration clock signal pins
3 of all of the memory devices such that configuration data is transmitted simultaneously from all of the
4 memory devices to the programmable device.

1 34. (currently amended) An apparatus comprising:
2 a programmable device; and
3 two or more memory devices, wherein:
4 the programmable device is connected simultaneously in parallel to each memory device
5 such that the programmable device is adapted to receive configuration data stored in the two or more
6 memory devices without transmitting the configuration data via a controller connected between any of
7 the memory devices and the programmable device, wherein the programmable device is adapted to
8 receive a different portion of the configuration data from each different memory device.

1 35. (currently amended) A method for configuring a programmable device, comprising:
2 simultaneously reading configuration data from two or more memory devices connected in
3 parallel to the programmable device without transmitting the configuration data via a controller
4 connected between any of the memory devices and the programmable device, wherein the programmable
5 device receives a different portion of the configuration data from each different memory device; and
6 configuring the programmable device using the configuration data.

1 36. (new) The invention of claim 1, wherein the different portions of the configuration data
2 are adapted to be simultaneously transmitted in parallel to the programmable device.

1 37. (new) The invention of claim 17, wherein the different portions of the configuration
2 data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 38. (new) The invention of claim 18, wherein the different portions of the configuration
2 data are simultaneously transmitted in parallel to the programmable device.

1 39. (new) The invention of claim 19, wherein the different portions of the configuration
2 data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 40. (new) The invention of claim 34, wherein the different portions of the configuration
2 data are adapted to be simultaneously transmitted in parallel to the programmable device.

1 41. (new) A programmable device comprising a Serial Peripheral Interface (SPI) adapted to
2 be connected to an SPI interface of at least one SPI serial memory device such that the programmable
3 device is adapted to receive configuration data stored in the SPI serial memory device without
4 transmitting the configuration data via a controller connected between the SPI serial memory device and
5 the programmable device, wherein the programmable device is adapted to receive instructions to ignore
6 data from an SPI serial memory device.

1 42. (new) The invention of claim 41, wherein the programmable device is adapted to
2 retrieve the instructions from the configuration data.